OBJECTIVE: RISC-V is an open source instruction set architecture (ISA). The offeror shall develop a RISC-V Digital Signal Processor (DSP) architecture using a true Harvard cache and bus architecture (completely separate instruction and data bus architecture).

DESCRIPTION: We are interested in RISC-V DSP architecture to create an open source DSP standard with preplanned expansion opportunities similar to the RISC-V design philosophy [1-5]. We are also interested in the benefits provided by a true Harvard architecture over a unified von Neumann architecture. A true Harvard machine can perform simultaneous program instruction and data memory operations. The cybersecurity benefits for completely separating (isolating) program instructions from data has been ignored by the computer industry.

The offeror shall develop a RISC-V DSP architecture using a true Harvard cache and bus architecture [6] (completely separate instruction and data bus architecture). We are not interested in a modified Harvard architecture [7] nor a von Neumann architecture [8]. The offeror shall develop a RISC-V DSP architecture which provides for fixed point and floating point complex multiply and add and other DSP related instructions with planned extensions for 64 bit and higher.

The offeror is required to meet the performance objectives (1)-(4) by comparing the performance of an equivalent RISC-V floating point microprocessor to the proposed RISC-V DSP. The only architecture differences between the RISC-V core and RISC-V DSP are the instruction extensions and architecture extensions to support DSP operations.

1. For a 256 by 256 complex double precision floating point matrix, and an 8 by 8 complex double precision floating point convolution kernel, demonstrate a 20 % higher performance.
2. For a 16k (1024*16) input sequence, and a 500 (or 501) tap double precision floating point, FIR Hilbert transform, demonstrate a 20 % higher performance.
3. For a 16k (1024*16) point double precision, floating point complex number FFT, demonstrate a 50% higher performance.
4. For a 64k (1024*64) point double precision, floating point complex number FFT, demonstrate 10% less energy used for the calculation.

Higher performance definition: 20 % higher performance means 20% less wall clock time to execute.

PHASE I: For the Phase I proposal, offeror shall describe the feasibility of developing a true Harvard RISC-V DSP architecture using a hardware/software co-design approach. The phase I proposal must address requirements (1)-(5). Proposals that do not meet the requirements will be deemed non-compliant and will not be reviewed. (1) Propose a co-design approach for RISC-V DSP architecture and DSP software extensions. (2) Propose DSP extensions for RISC-V architecture and a path forward to standardize the proposed extensions. (3) A design concept to achieve the performance metrics in the description section. (4) Describe potential Army, DoD, and commercial applications; and (5) Provide a business model to market (a) the proposed open source RISC-V DSP and (2) if the offeror chooses to develop a closed source version a second marketing plan. For the phase I effort, the offeror shall demonstrate the feasibility of developing a RISC-V DSP architecture using a true Harvard machine architecture. (1) Develop models, simulations, prototypes, etc. to determine technical feasibility of developing a true Harvard architecture RISC-V DSP. (2) Deliver a System Architecture Report describing RISC-V DSP architecture. (3) Publish a proposed, open standard for RISC-V DSP ISA and Harvard cache and bus Architecture. (4) Write a report describing the benefits [9] and costs of a true Harvard architecture over a von Neumann architecture covering (1) higher bandwidth, (2) better isolation between instructions and data, (3) more parallelism, et al. The intention of this report is to (1) illustrate to the microprocessor community the parallel performance advantages of a Harvard architecture and (2) to show to the cybersecurity community that the isolation provided by a Harvard architecture is significantly better than a von Neumann architecture.

PHASE II: Phase II: Offeror shall develop a RISC-V DSP based on offeror’s proposal and phase I effort. The offeror shall demonstrate RISC-V DSP for an Army application (like Joint Multi-Role Technology Demonstrator [10]). The Offer shall propose potential applications for a system demonstration and implement an application with government concurrence. Offeror shall create an open source RISC-V DSP version in a standard hardware description language (VHDL, Verilog, SystemC, etc.) and provide an open source license. The offeror shall publish an open source architecture document covering RISC-V DSP (VHDL, Verilog, SystemC, etc.) code and system development board. Offeror is free to develop another version which may be fully proprietary. Offeror shall deliver 2 prototype systems.
to the government point of contact for test and evaluation with all software tools and licenses (if required), and hardware description language code(s) and software to build and use the system. Offeror shall provide 2 days of on-site training for the system.

PHASE III DUAL-USE APPLICATIONS: Offeror will develop and market RISC-V DSP based on phase II development work and marketing plan from phase I. Offeror may target low power applications or high end DSP market. Offeror will integrate RISC-V DSP into an Army Aviation or Missile subsystem currently under development or via technology refresh.

REFERENCES:
6. en.wikipedia.org/wiki/Harvard_architecture
7. en.wikipedia.org/wiki/Modified_Harvard_architecture
8. en.wikipedia.org/wiki/Von_Neumann_architecture
10. defenseinnovationmarketplace.mil/resources/JMR_AMRDEC01.pdf

KEYWORDS: RISC-V, digital signal processing, Harvard machine, Hardware/Software Co-design