INTRODUCTION

The Defense Microelectronics Activity (DMEA) SBIR/STTR Program is implemented, administrated, and managed by the DMEA Office of Small Business Programs (OSBP). If you have any questions regarding the administration of the DMEA SBIR/STTR Program, please contact the DMEA SBIR/STTR Program Manager (PM), Mr. Greg Davis, at osd.mcclellan-park.dmea.list.smbus@mail.mil.

For general inquiries or problems with electronic submission, contact the DOD SBIR/STTR Help Desk at 1-703-214-1333 or email dodsbirsupport@reisystems.com between 9:00 am to 5:00 pm ET. For questions about the topic during the pre-release period (Please refer to the DoD 21.1 SBIR BAA for dates), contact the Technical Point of Contact (TPOC) listed under each topic on the DOD SBIR/STTR Innovation Portal (DSIP) website (https://www.dodsbirsttr.mil/submissions/login) prior to the Open phase of the DOD SBIR Program Broad Agency Announcement (BAA) FY 21.1. The Topic Q&A (formerly SITIS) will be open to questions during pre-release and close to new questions two weeks prior to the announcement close date. More information on Topic Q&A, can be found at https://www.dodsbirsttr.mil/topics-app/. Information regarding the DMEA mission and programs can be found at https://www.dmea.osd.mil/.

PHASE I GUIDELINES

DMEA intends for Phase I to be only an examination of the merit of the concept or technology that still involves technical risk, with a cost not exceeding $167,500 (excludes Discretionary Technical and Business Assistance (TABA) amount).

A list of the topics currently eligible for proposal submission is included in this section followed by full topic descriptions. These are the only topics for which proposals will be accepted at this time. The topics are directly linked to DMEA’s core research and development requirements.

Please ensure that your e-mail address listed in your proposal is current and accurate. DMEA cannot be responsible for notification to companies that change their mailing address, e-mail address, or company official after proposal submission.

PHASE I PROPOSAL SUBMISSION

Read the DOD SBIR Program BAA FY 21.1 for detailed instructions on proposal format and program requirements. When you prepare your proposal submission, keep in mind that Phase I should address the feasibility of a solution to the topic. Only UNCLASSIFIED proposals will be entertained.

The technical period of performance for the Phase I effort should be no more than six (6) months. DMEA will evaluate and select Phase I proposals using the evaluation criteria contained in Section 6.0 of the DOD SBIR Program BAA FY 21.1 Preface Instructions. Due to limited funding, DMEA reserves the right to limit awards under any topic, and only proposals considered to be of superior quality will be funded.

DMEA does not accept Phase I proposals exceeding $167,500. DMEA will conduct a price analysis to determine whether cost proposals, including quantities and prices, are fair and reasonable. Contractors should expect that cost proposals will be negotiated.
If you plan to employ NON-U.S. citizens in the performance of a DMEA SBIR contract, please identify these individuals in your proposal as specified in Section 5.4.c(8) of the DOD SBIR Program BAA FY 21.1.

It is mandatory that the ENTIRE Technical Volume, DOD Proposal Cover Sheet and Cost Volume are submitted electronically through the DOD SBIR website at https://www.dodsbirstr.mil/submissions/. The DOD proposal submission site submission will lead you through the process for submitting your technical proposal and all of the sections electronically. Each of these documents is submitted separately through the website. If you have any questions or problems with the electronic proposal submission, contact the DOD SBIR/STTR Help Desk at 703-214-1333 or email dodsbirstsupport@reisystems.com. DMEA established page limits for the Technical and Cost Volumes are 20 pages each.

A Company Commercialization Report (CCR) is required to be submitted with Phase I proposals in response to the DMEA 21.1 SBIR topics. Firms must complete this report by logging into the firm’s account on SBIR.gov and starting a new Company Commercialization Report. Once the firm completes and submits this report within the SBIR.gov website, it should download a PDF copy and include the PDF as an upload in Volume 4: CCR of its DSIP proposal submission. Please refer to the DoD 21.1 SBIR BAA for full details.

Volume 6: Fraud, Waste and Abuse (FWA) training is required for Phase I and Direct to Phase II proposals. Please refer to the DoD 21.1 SBIR BAA for full details.

Your proposal submission must be submitted via the submission site on or before the date published in the DoD 21.1 SBIR BAA.

Proposal submissions that are not complete or that are received after the closing date and time will not be considered for award.

**PHASE II GUIDELINES**

Phase II is the prototype/demonstration of the technology that was found feasible in Phase I. DMEA encourages, but does not require, partnership and outside investment as part of discussions with DMEA sponsors for potential Phase II efforts.

Phase II proposals may be submitted for an amount not to exceed $1,100,000 (excludes Discretionary Technical and Business Assistance (TABA) amount). The technical period of performance for the Phase II effort should be no more than twenty-four (24) months.

**PHASE II PROPOSAL SUBMISSION**

Phase I awardees may submit a Phase II proposal without invitation not later than sixty (60) calendar days following the end of the Phase I contract. The Phase II proposal submission instructions are identified in the Phase I contract, Part I – The Schedule, Section H, Special contract requirements, “SBIR Phase II Proposal Submission Instructions.”

All Phase II proposals must have a complete electronic submission. Complete electronic submission includes the submission of Cover Sheet, Cost Volume, the entire Technical Volume, and any appendices via the DOD submission site (https://www.dodsbirstr.mil/submissions/). The DOD proposal submission site will lead you through the process for submitting your technical volume and all of the sections electronically. Each of these documents is submitted separately through the website. Your proposal must be submitted via the submission site on or before the DMEA-specified deadline or it will not be...
considered for award. DMEA established page limits for the Technical and Cost Volumes are 20 pages each.

A Company Commercialization Report (CCR) is required to be submitted with Phase II proposals in response to the DMEA 21.1 SBIR topics. Firms must complete this report by logging into the firm’s account on SBIR.gov and starting a new Company Commercialization Report. Once the firm completes and submits this report within the SBIR.gov website, it should download a PDF copy and include the PDF as an upload in Volume 4: CCR of its DSIP proposal submission. Please refer to the DoD 21.1 SBIR BAA for full details.

The technical period of performance for the Phase II effort should be no more than twenty-four (24) months. DMEA will evaluate Phase II proposals based on the Phase II evaluation criteria listed in Section 8.0 of DOD SBIR Program BAA FY 21.1 Preface. Please reference the DOD SBIR Submission site FAQs for more information on generating Phase II proposals. Due to limited funding, DMEA’s ability to award any Phase II, regardless of proposal quality or merit, is subject to availability of funds. Please ensure that your proposal is valid for 120 days after submission, and any extension to that time period will be requested by the contracting officer.

Any follow-on Phase II proposal (i.e., a second Phase II subsequent to the initial Phase II effort) shall be initiated by the Government Technical Point of Contact for the initial Phase II effort and must be approved by the DMEA SBIR/STTR Program Manager in advance.

COST VOLUME GUIDELINES

The on-line cost volume for Phase I and Phase II proposal submissions must be at a level of detail that would enable DMEA personnel to determine the purpose, necessity, and reasonability of each cost element. Provide sufficient information (a. through h. below) on how funds will be used if the contract is awarded. Include the itemized cost volume information (a. through h. below) as an appendix in your technical proposal. The itemized cost volume information (a. through h. below) will not count against the 20-page limit on Phase I and II proposal submissions.

a. Special Tooling and Test Equipment and Material: The inclusion of equipment and materials will be carefully reviewed relative to need and appropriateness of the work proposed. The purchase of special tooling and test equipment must, in the opinion of the Contracting Officer, be advantageous to the government and relate directly to the specific effort. They may include such items as innovative instrumentation and/or automatic test equipment. Title to property furnished by the Government or acquired with Government funds will be vested with the DOD Component; unless it is determined that transfer of the title to the contractor would be more cost effective than recovery of the equipment by the DOD Component.

b. Direct Cost Materials: Justify costs for materials, parts, and supplies with an itemized list containing types, quantities, price, and where appropriate, purposes.

c. Other Direct Costs: This category of costs includes specialized services such as machining or milling, special testing or analysis, costs incurred in obtaining temporary use of specialized equipment. Proposals, which include teased hardware, must provide an adequate lease versus purchase justification or rationale.

d. Direct Labor: Identify key personnel by name if possible or by labor category if specific names are not available. The number of hours, labor overhead and/or fringe benefits and actual hourly rates for each individual are also necessary.
e. Travel: Travel costs must relate to the needs of the project. Break out travel cost by trip, with the number of travelers, airfare, and per diem. Indicate the destination, duration, and purpose of each trip.

f. Cost Sharing: Cost sharing is permitted. However, cost sharing is not required, nor will it be an evaluation factor in the consideration of a proposal.

g. Subcontracts: Involvement of university or other consultants in the planning and/or research stages of the project may be appropriate. If the offeror intends such involvement, describe the involvement in detail and include information in the cost proposal. The proposed total of all consultant fees, facility leases, or usage fees and other subcontract or purchase agreements may not exceed one-third of the total contract price or cost, unless otherwise approved in writing by the Contracting Officer. Support subcontract costs with copies of the subcontract agreements. The supporting agreement documents must adequately describe the work to be performed (i.e., Cost Volume). At the very least, a statement of work with a corresponding detailed cost volume for each planned subcontract must be provided.

h. Consultants: Provide a separate agreement letter for each consultant. The letter should briefly state what service or assistance will be provided, the number of hours required, and the hourly rate.

**DMEA SBIR PHASE II ENHANCEMENT PROGRAM**

To encourage transition of SBIR into DOD systems, DMEA has a Phase II Enhancement policy. DMEA’s Phase II Enhancement program requirements include: up to one-year extension of existing Phase II, and up to $550,000 matching SBIR funds. Applications are subject to review of the statement of work, the transition plan, and the availability of funding. DMEA will generally provide the additional Phase II Enhancement funds by modifying the Phase II contract.

**DISCRETIONARY TECHNICAL AND BUSINESS ASSISTANCE (TABA)**

DMEA does not provide Discretionary Technical and Business Assistance (TABA).

**PHASE I PROPOSAL SUBMISSION CHECKLIST:**

All of the following criteria must be met or your proposal will be REJECTED.

1. Your Technical Volume, the DOD Cover Sheet, the DOD Company Commercialization Report (required even if your firm has no prior SBIRs), and the Cost Volume have been submitted electronically through DSIP on or before the date published in the DoD 21.1 SBIR BAA.

2. The Phase I proposal does not exceed $167,500 (excludes Discretionary Technical and Business Assistance (TABA) amount).
<table>
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TITLE: SiC BiCMOS Platform Development

RT&L FOCUS AREA(S): Microelectronics

TECHNOLOGY AREA(S): Electronics

OBJECTIVE: To develop a BiCMOS platform utilizing SiC wafer to achieve high temperature operation and high voltage/power integration.

DESCRIPTION: As a result of almost four decades long investment on SiC technology by DoD and technical breakthroughs achieved by private sectors, affordable high-voltage SiC MOSFETs debut in the market recently [1][2]. The 650+V SiC MOSFETs become popular switching devices in data center, renewable energy, and even electric vehicle applications thanks to excellent energy efficiency and reduction in the power conversion system size and weight.

While discrete SiC power devices are successfully commercialized, separate efforts to develop SiC integrated circuits (ICs), that can be used in high temperature and high radiation environments, have continued for a decade. Those ICs were mostly based on non-CMOS, (i.e. bipolar transistor [3], MESFET [4] and JFET [5][6]) due to many technical barriers in SiC CMOS technology such as low channel mobility, uneven performance of NMOS vs. PMOS, forming resistive ohmic contacts, and gate oxide reliability.

More recently, advantages such as convenient digital circuit design using standard libraries and low power consumption of CMOS configuration drive big corporations [7][8] and small businesses [9][10] to jump into the SiC CMOS IC development competition. Despite these aspirations and effort, decent SiC CMOS technology development will not be easy to overcome the fundamental material properties of SiC including high gate oxide/SiC interface states.

The goal of this solicitation is to develop and demonstrate a SiC BiCMOS platform that can be applied up to 300°C ambient temperature. Base materials for this solicitation include, but are not limited to bulk or epitaxial SiC wafer, Si/SiC direct bonding (Si/SiC DB) wafer, or Si-epitaxial grown on SiC substrate (Si-epi/SiC) wafer.

PHASE I: Perform a Feasibility Study that addresses the gate oxide related parameters such as channel mobility, gate tunneling current, time-dependent dielectric breakdown (TDDB), bias temperature instability (BTI), and yield (extrinsic failure rate). Key parameters related to the gate oxide should meet requirements as below.

- NMOSFET channel mobility > 50 cm²/V·s
- PMOSFET channel mobility > 10 cm²/V·s
- Threshold voltage shift (for NMOSFET and PMOSFET) < ±500 mV at bias-temperature stress during mean time to failure

When Si/SiC DB or Si-epi/SiC wafers are used, Si/SiC interface and across-wafer uniformity should be characterized by various imaging tools and spectroscopy. All junction combinations between (n and p-type) Si and (n and p-type) SiC have to be characterized electrically to monitor the ohmic and p-n junction behavior. Key parameters related to SiC/Si interface should meet requirements as below.

- Void free and continuous SiC/Si interface throughout entire wafer
- Bonding interface thickness (thickness of SiO₂, amorphous Si or carbon rich region) < 10 nm
- Bonding interface state density < 1x10¹² eV⁻¹cm²
If those key parameters are not met the requirements, detailed plans for improvement of those reliability and performance parameters during phase II must be proposed.

PHASE II: Prototype deliveries of phase II are development of wafer fabrication process and Process Design Kit (PDK). Based on the process, statistical data of critical parameters and reliability (mostly gate oxide related) data for technology qualification are to be reported. For CMOS transistors and high-voltage LDMOS, BSIM (or BSIM equivalent or modified BSIM) models incorporating statistical data shall be included in the PDK.

During the first year of phase II, TCAD simulations on n-channel and p-channel LDMOS (45V, 120V, and 650V) and other active and passive devices are necessary to define device architecture, dimension, and doping profile. Wafer processing modules (gate/field oxidation, isotropic/anisotropic etch, implant, activation/annealing, and contact/interconnect/pad metallization) on SiC or Si/SiC wafer should be developed. When SiC bulk or epitaxial wafer is used, process development should be carried out including efforts to improve gate oxide integrity, PMOS transconductance, source/drain/body ohmic contacts, and passive components temperature dependency. When Si/SiC wafer is used, wafer bonding or Si epitaxial processes, which can reproduce Si/SiC wafers, must be identified. All the process modules should be matured and stabilized.

During the second year of phase II, all BiCMOS platform device components, which comprise of core logic CMOS transistors, analog MOSFETs (for current mirrors, differential pairs, etc), bipolar transistors, passives (diffusion and poly resistors, gate oxide or MIM capacitors), and high-voltage (45V, 120V, and 650V) LDMOSs are to be fabricated on a single die, and characterized at temperature range over -55°C to 300°C. Performance of those devices are to be improved/optimized though multiple test vehicles.

PHASE III DUAL USE APPLICATIONS: Continuous efforts may be needed to further stabilize the process flow which ensures product reliability to embody strong business case. Variations of the baseline flow are to be developed, for example, different technology nodes, gate oxide thickness, and LDMOS voltage ratings. The BiCMOS platforms could be utilized for smart power IC production, second source manufacturing or licensing.

SiC wafer platform is advantageous for high-temperature and radiation hardened ICs (when semi-insulating SiC substrates are used). On the other hand, Si/SiC wafer platform allows hybrid integration of high density Si CMOS logic and SiC high-voltage power devices. The platform could take advantage of Si/SiC heterojunction properties to enhancing LDMOS performance [11][12].

Those platforms are highly attractive to NASA’s space programs, Air Force’s aircrafts, Army’s combat electric vehicles and nuclear facilities where harsh environment electronics are required. Analog Devices’ AD8229 and ADXL206 are notable commercialized Si based products available in the market targeting oil/gas drilling, aerospace, and geothermal applications under 200°C ambient temperature. Many defense and civilian industries are anticipating SiC IC products that can operate above the Si temperature limit.

The Si/SiC DB wafer has not been commercialized simply due to lack of demand. If the Si/SiC platform development is successful, it would create demand for Si/SiC DB wafers as a base material for the BiCMOS IC production. Therefore, Si/SiC wafer manufacturing business will be a promising derivative from the platform development.

POTENTIAL VALUE TO DoD: Because weapon systems operate under unexpected theatrical conditions, the systems have to be small, light, and energy efficient to meet size/weight/power (SWaP) goal of DoD.
SiC BiCMOS ICs help to achieve the goals by making electronic modules simple, highly functional, and intelligent.

REFERENCES:

11. Baoxing Duan, “Si/SiC heterojunction lateral double-diffused metal oxide semiconductor field effect transistor with breakdown point transfer (BPT) terminal technology,” Micro & Nano Letters, 2019
12. Qi Li, “Novel SiC/Si heterojunction LDMOS with electric field modulation effect by reversed L-shaped field plate,” Results in Physics, 2020

KEYWORDS: SiC, BiCMOS, Si/SiC heterojunction, integrated circuit, high-temperature, high-voltage
The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), 22 CFR Parts 120-130, which controls the export and import of defense-related material and services, including export of sensitive technical data, or the Export Administration Regulation (EAR), 15 CFR Parts 730-774, which controls dual use items. Offerors must disclose any proposed use of foreign nationals (FNs), their country(ies) of origin, the type of visa or work permit possessed, and the statement of work (SOW) tasks intended for accomplishment by the FN(s) in accordance with section 3.5 of the Announcement. Offerors are advised foreign nationals proposed to perform on this topic may be restricted due to the technical data under US Export Control Laws.

RT&L FOCUS AREA(S): Microelectronics

TECHNOLOGY AREA(S): Battlespace, Electronics, Sensors

OBJECTIVE: Develop a tool for automated, procedural planar serial sectioning of semiconductor microelectronic devices.

DESCRIPTION: Serial sectioning Integrated Circuits (ICs) to perform Failure Analysis (FA), Fault Isolation (FI), Reverse Engineering (RE), and Design Validation (DV) is time-consuming and repetitive work that is well suited for human-robot collaboration and robotic automation. Frontside, backside, and crosswise serial sectioning of IC samples often requires operators to maintain a serial sectioning precision to within less than twenty nanometers for multiple hours or days, often leading to operator fatigue and error. The wet chemistry, polishing slurries and pressurized nitrogen flows involved in serial sectioning do not easily lend themselves to bench-top systems. A larger, human-scale processing space oriented around an extended robotic arm with the ability to transition samples between acid baths of etchant, colloidal silica polishing slurries, liquid-soaked cleaning pads, sonicating baths of cleaning solvents, and compressed nitrogen gasses for drying samples is a realistic approach to both automating these processes and to minimizing the cost of maintaining equipment. The physical separation between each serial sectioning process that a robotic arm affords will prevent cross-contamination of materials, allow ease of access for preventative maintenance and routine equipment cleaning, and prevent liquids and corrosives from damaging mechanical and electrical equipment. A robotic arm also allows for the possibility of automatically inserting samples into a Scanning Electron Microscope (SEM) after each successive serial sectioning step. Current technology is limited to automatic frontside, backside, and crosswise serial sectioning to within accuracies of approximately one micron. Defense Microelectronics Activity needs the capability to do this to within tens of nanometers. While humans are able to perform all three of these processes, repeatability between sample preparation is often inconsistent, and both the great length of time it takes to perform coupled with limited numbers of personnel makes it impossible to validate the designs of and perform failure analysis on the large quantity of microelectronics employed by DoD. It is critical to national security and to the work being done by multiple DoD initiatives across different agencies that these processes become automated in the near future.

PHASE I: Feasibility study of automatic serial sectioning an IC to an arbitrary metal layer in a planar manner that results in all vias being present, along with a relatively uniform interlayer dielectric material (ILD), and all metal lines beneath it. Having all three of these present in a single image: vias, the ILD to hold the vias in place, and the metal lines beneath the ILD is the first preliminary benchmark of the automatic serial sectioning system. The following requirements should be met:

1) Material removal with an accuracy of less one-hundred nanometers across a one square centimeter IC with reference to the initial planar surface of the IC, or less than 0.0006° tilt.
2) Highly perpendicular crosswise serial sectioning to within 90°±0.0006°.
3) Serial-sectioning to a target location with accuracy of less than a micron.
4) Microscope images should be taken while serial-sectioning. All vias and metal lines of the layer of interest should be present at time of imaging, and the microscope should be capable of imaging these vias and metal lines up to 500x magnification.

5) A study should be done on how to make all equipment and machinery self-contained, requiring no external plumbing, drainage, or ventilation. Details should be provided on how this will be achieved in Phase II.

6) Detailed recipes, stating rates or times taken to serial section, and clean IC samples should be provided. All equipment, chemicals, materials, and supplies employed in the process should be stated.

7) DMEA users of the tool should have the full ability to program the machine to suit their needs. The software should include flexibility to modify serial sectioning recipes and parameters.

8) Detailed plans of all mechanical parts designed for this contract should be furnished to DMEA in original digital format.

Deliver a feasibility report of research and innovation, including a list of possible components, a storyboard of software that will control the tool and a program plan for system development. If any of the above restraints cannot be adhered to, the report must include relevant research and rationale. If adhering to the above constraints is possible, but not financially feasible, the report must include relevant research and rationale.

PHASE II: Based on the aforementioned study and applicable innovation,

1) Produce a fully functioning self-contained prototype that adheres to all the constraints listed in Phase I.

2) Test the prototype and deliver along with at least (3) samples for each application, for a total of (9) samples. The applications are: Frontside, backside, and crosswise serial sectioning. The samples should all be the same device (to be determined during Phase I) and should show the process repeatability between both samples.

3) Deliver a complete Bill of Materials (BOM), including all part numbers used, manufacturers, quantities, technical datasheets, facility requirements, and deliver CAD files and digital designs of all mechanical parts designed for this SBIR.

4) Provide multiple images showing individual IC metal layers, along with ILD, and all vias intact showing that the process is repeatable. For example, only seven of these types of images for a seven metal layer device are required to obtain all data of the entire integrated circuit design layout. Due to time constraints, this requirement is not mandatory, although this is one of the intended purposes of the equipment. It will do a great service to the reputed capability of the system if it demonstrates that it can validate the design of an entire IC by frontside serial sectioning.

PHASE III DUAL USE APPLICATIONS: There may be opportunities for further development of this system for use in a specific military or commercial application. During a Phase III program, offerors may refine the performance of the design and produce pre-production quantities for evaluation by the Government.

The Robotic Microelectronic Planar Serial Sectioning would be applicable to both commercial and
government semiconductor device research and FA. Government applications include FA, FI, DV and RE of semiconductors. Commercial applications include FA and FI of semiconductors.

POTENTIAL VALUE TO DoD: High throughput serial sectioning of integrated circuits for the purposes of failure analysis, fault isolation, reverse engineering, design validation and counterfeit inspection is critical to national security. Given the sheer quantity of microelectronics employed by DoD, automation is a realistic approach to performing these tasks at scale.

REFERENCES:


KEYWORDS: Serial Sectioning, Failure Analysis, Reverse Engineering, Microelectronics, Sample Preparation, Design Validation, Fault Isolation, Counterfeit Inspection